ABSTRACT

A semiconductor storing device can access a plurality of addresses simultaneously without increasing a circuit area and a wiring area. A row of memory cells is selected by two stages of a word line and a division word line. An address is specified by X[i:0], Y[j:0], and Z[k:0]. Two roots of selection signals are alternately provided to division word line selectors arranged in one memory array. One of two roots of the selection signals is enabled to select the division word line selector. Eight roots of the selection signals in the entire semiconductor storing device are enabled to access eight addresses simultaneously.